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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/523,379
Filing Date: December 14, 2005
Appellant(s): CHILDS ET AL.

Gregory L. Thorne
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/10/2008 appealing from the Office action mailed 7/11/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

To the best of the Examiners' knowledge, there are no related appeals or interferences.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6734636	Sanford	6-2002
2001/0002703	Koyama	11-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanford et al. (United States Patent 6,734,636), hereinafter referenced as Sanford, in view of Koyama (United States Patent Application Publication 2001/0002703), hereinafter referenced as 703.

Regarding claim 1, Sanford discloses an active matrix electroluminescent display device comprising an array of display pixels, each pixel comprising: an electroluminescent display element; an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line; a storage capacitor between the anode of the display.element and the gate of the first drive transistor; and an amorphous silicon or microcrystalline silicon second drive NMOS transistor for supplying a holding voltage to the anode of the display element. Specifically Sanford discloses an OLED display with pixels where each pixel comprises:

an electroluminescent display element or OLED 320 exhibited in figure 3;

an amorphous silicon drive NFET Q303 connected between the anode of the OLED 320 and a power supply line exhibited in figure 3 and disclosed in column 1 lines 13-40.

a storage capacitor CS310 between the anode of the OLED 320 and the gate of the first drive transistor Q303 exhibited in figure 3;

an amorphous silicon drive NFET Q302 for supplying a holding voltage to the anode of the OLED 320 exhibited in figure 3 and disclosed in column 1 lines 13-40 and in column 6 lines 10-67.

However Sanford fails to disclose a transistor directly connected to the anode of the display element.

However the examiner maintains that it was well known in the art to provide a transistor directly connected to the anode of the display element, as taught by 703.

In a similar field of invention 703 discloses a second transistor (1409) that is directly connected to the anode of the display element (paragraph 67; paragraph 118; paragraph 124; paragraphs 155-158; figure 4A; figures 7A-7B).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford by specifically providing a transistor directly connected to the anode of the display element for the purpose of improving the quality of the display by compensating for any decrease in the number of gradations (paragraphs 43-45).

Regarding claim 2, Sanford and 703, the combination discloses everything as applied above, in addition Sanford discloses wherein the second drive transistor is connected between the power supply line and the anode of the display element. Specifically Sanford discloses that the second drive transistor Q302 is connected between the power supply line and the anode of the OLED 320 exhibited in figure 3.

Regarding claim 5, Sanford and 703, the combination discloses everything as applied above (see claim 1), in addition Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Regarding claim 5, Sanford and 703, the combination discloses everything as applied above (see claim 2), in addition Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Regarding claim 15, Sanford and 703, the combination discloses everything as applied above, in addition Sanford discloses wherein a cathode of the EL display

element is directly connected to a relative ground or low voltage (column 6 lines 22-48; figure 3).

Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanford in view of 703 and further in view of Koyama et al. (United States Patent Application Publication 2001/0043168), hereinafter referenced as Koyama.

Regarding claim 3, Sanford and 703, the combination discloses everything as applied above, however the combination fails to disclose wherein the second drive transistor is connected between a second power supply line and the anode of the display element.

However the examiner maintains that it was well known in the art to provide wherein the second drive transistor is connected between a second power supply line and the anode of the display element, as taught by Koyama.

In a similar field of invention Koyama discloses a display device. Further Koyama discloses that a second drive transistor 4406 is connected between a second power supply line VY1 and the anode of the display element 4414 disclosed in paragraph 131 and in paragraph 133 and in paragraph 149 and exhibited in figure 2.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford and 703 with Koyama by specifically providing wherein the second drive transistor is connected between a second power supply line and the anode of the display element for the purpose of allowing each pixel

to use multiple power lines to decrease the length of power lines required for the display.

Regarding claim 4, Sanford, 703 and Koyama, the combination discloses everything as applied above (see claim 3), further Koyama discloses that a second drive transistor 4406 is connected between a second power supply line VY1 and the anode of the display element 4414 where the second power supply line is shared between a row of pixels disclosed in paragraph 149 and exhibited in figure 2.

Regarding claim 5, Sanford, 703 and Koyama, the combination discloses everything as applied above (see claim 3), in addition Sanford discloses that the gate of the first drive transistor is coupled to a data signal line through an address transistor. Specifically Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Regarding claim 5, Sanford, 703 and Koyama, the combination discloses everything as applied above (see claim 4), in addition Sanford discloses that the gate of the first drive transistor is coupled to a data signal line through an address transistor. Specifically Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Regarding claim 6, Sanford and 703, the combination discloses everything as applied above, however the combination fails to disclose wherein the data signal line comprises a column conductor shared between pixels in a column of the array.

However the examiner maintains that it was well known in the art to provide wherein the data signal line comprises a column conductor shared between pixels in a column of the array, as taught by Koyama.

In a similar field of invention Koyama discloses a display device. Further Koyama discloses that the data signal line Sn is a column conductor shared between the pixels of a column of the array of pixels disclosed in paragraph 149 and exhibited in figure 2.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford and 703 with Koyama by specifically providing wherein the data signal line comprises a column conductor shared between pixels in a column of the array for the purpose of allowing the pixels to be arranged in rows and columns to display an image.

Regarding claim 7, Sanford, 703 and Koyama, the combination discloses everything as applied above, in addition 703 discloses that the gate of the address transistor (1401) is coupled to a row conductor shared between pixels in a row of the array (figures 2-3; figure 4A).

Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanford in view of 703 and further in view of Yamazaki et al. (United States Patent Application Publication 2002/0105040), hereinafter referenced as Yamazaki.

Regarding claim 6, Sanford and 703, the combination discloses everything as applied above, further Sanford discloses first and second drive transistors (figures 2-3), however the combination fails to disclose microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm-140 nm in an amorphous silicon matrix.

However the examiner maintains that it was well known in the art to provide microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm-140 nm in an amorphous silicon matrix, as taught by Yamazaki.

In a similar field of invention Yamazaki discloses microcrystalline silicon TFTs comprising silicon crystallites of size 20 nm to 70 nm which is within the range of 40 nm-140 nm in an amorphous silicon matrix (paragraphs 43-44; paragraph 82; paragraph 144; figure 1; figures 2A-2B).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford and 703 with Yamazaki by specifically providing microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm-140nm in an amorphous silicon matrix for the purpose of producing a display with TFTs easily and reliably (paragraph 11).

Claims 9-13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanford in view of 703 and further in view of Shimoda (United States Patent 6,809,706), hereinafter referenced as Shimoda.

Regarding claim 9, Sanford discloses a method of driving the pixels of an active matrix electroluminescent display device comprising an array of display pixels each having an electroluminescent display element, the method comprising: holding the voltage across the display element by applying a holding voltage through a first amorphous silicon or microcrystalline silicon NMOS transistor; while holding the voltage across the display element, storing a desired gate-source voltage on a storage capacitor connected between the gate and source of the second transistor, the gate-source voltage corresponding to a desired source-drain current for driving the display element; removing the holding voltage from the display element; and driving the desired source-drain current through the electroluminescent display element. Specifically Sanford discloses a method for driving an EL display with pixels with EL display elements comprising:

holding the voltage across an OLED 320 by applying a voltage through a first amorphous silicon NMOS transistor Q302 disclosed in column 6 lines 16-35 and exhibited in figure 3.

storing a desired gate-source voltage on a storage capacitor Cs310 connected between the gate and source of the second transistor Q303, the gate-source voltage

corresponding to a desired source-drain current for driving the OLED 320 disclosed in column 6 lines 16-67 and exhibited in figure 3.

removing the voltage from the OLED 320 disclosed in column 6 lines 30-35.

driving the desired source-drain current through the OLED 320 disclosed in column 6 lines 41-48.

However Sanford fails to disclose directly connected to an anode of the electroluminescent display element, and the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor.

However the examiner maintains that it was well known in the art to provide directly connected to an anode of the electroluminescent display element, and the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor, as taught by 703 and Shimoda, respectively.

In a similar field of invention 703 discloses a second transistor (1409) that is directly connected to the anode of the display element (paragraph 67; paragraph 118; paragraph 124; paragraphs 155-158; figure 4A; figures 7A-7B).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford with 703 by specifically providing a transistor directly connected to the anode of the display element for the purpose of improving the quality of the display by compensating for any decrease in the number of gradations (paragraphs 43-45).

In a similar field of invention Shimoda discloses a drive circuit for a display device. Shimoda further discloses that a voltage supplied from a transistor Tr1 to a capacitor C1 holds the gate-source voltage of a second NMOS transistor Tr2 exhibited in figure 12A and disclosed in column 4 lines 19-20 and in column 7 lines 61-64.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford with Shimoda by specifically providing the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor for the purpose of allowing the OLED to display a portion of an image properly.

Regarding claim 10, Sanford, 703 and Shimoda, the combination discloses everything as applied above (see claim 9), further Sanford discloses wherein the desired source-drain current is driven through the second transistor by applying a first power supply voltage to the second transistor. Specifically Sanford discloses that the desired source-drain current is driven through the second transistor Q303 by applying a first power supply voltage Vdd to the transistor disclosed in column 6 lines 34-48.

Regarding claim 11, Sanford, 703 and Shimoda, the combination discloses everything as applied above (see claim 10), further Sanford discloses wherein the first power supply voltage is not applied to the second transistor while the voltage across the display element is held. Specifically Sanford discloses that the first power supply voltage Vdd is not applied to the second transistor Q303 while the voltage across the OLED is held constant disclosed in column 6 lines 30-34.

Regarding claim 12, Sanford, 703 and Shimoda, the combination discloses everything as applied above (see claim 11), further Sanford discloses wherein the first power supply voltage and the holding voltage are provided by a shared power supply line. Specifically Sanford discloses that first power supply voltage and the holding voltage on the capacitor Cs310 are provided by a shared power supply line Vdd exhibited in figure 3 and disclosed in column 6 lines 34-38 and in column 4 lines 58-62.

Regarding claim 13 (as dependent from claim 9), Sanford, 703 and Shimoda, the combination discloses everything as applied above (see claim 9), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done by coupling data from a data signal line 340 to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Regarding claim 13 (as dependent from claim 10), Sanford, 703 and Shimoda, the combination discloses everything as applied above (see claim 10), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done by coupling data from a data signal line 340 to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Regarding claim 13 (as dependent from claim 11), Sanford, 703 and Shimoda, the combination discloses everything as applied above (see claim 11), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done by coupling data from a data signal line 340 to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Regarding claim 13 (as dependent from claim 12), Sanford, 703 and Shimoda, the combination discloses everything as applied above (see claim 12), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done by coupling data from a data signal line 340

to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Regarding claim 16, Sanford, 703 and Shimoda, the combination discloses everything as applied above, in addition Sanford discloses wherein a cathode of the EL display element is directly connected to a relative ground or low voltage (column 6 lines 22-48; figure 3).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanford in view of 703 and further in view of Yamazaki.

Regarding claim 14, Sanford discloses an OLED display with pixels where each pixel comprises:

an electroluminescent display element or OLED 320 exhibited in figure 3;

an amorphous silicon drive NFET Q303 connected between the anode of the OLED 320 and a power supply line exhibited in figure 3 and disclosed in column 1 lines 13-40.

a storage capacitor CS310 between the anode of the OLED 320 and the gate of the first drive transistor Q303 exhibited in figure 3;

an amorphous silicon drive NFET Q302 for supplying a holding voltage to the anode of the OLED 320 exhibited in figure 3 and disclosed in column 1 lines 13-40 and in column 6 lines 10-67, where the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in

column 6 lines 10-67, the first and second drive transistors are TFTs exhibited in figure 3.

However Sanford fails to disclose a transistor directly connected to the anode of the display element and microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm-140 nm in an amorphous silicon matrix.

However the examiner maintains that it was well known in the art to provide a transistor directly connected to the anode of the display element and microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm-140 nm in an amorphous silicon matrix, as taught by 703 and Yamazaki, respectively.

In a similar field of invention 703 discloses a second transistor (1409) that is directly connected to the anode of the display element (paragraph 67; paragraph 118; paragraph 124; paragraphs 155-158; figure 4A; figures 7A-7B).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford by specifically providing a transistor directly connected to the anode of the display element for the purpose of improving the quality of the display by compensating for any decrease in the number of gradations (paragraphs 43-45).

In a similar field of invention Yamazaki discloses microcrystalline silicon TFTs comprising silicon crystallites of size 20 nm to 70 nm which is within the range of 40 nm-140 nm in an amorphous silicon matrix (paragraphs 43-44; paragraph 82; paragraph 144; figure 1; figures 2A-2B).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford and 703 with Yamazaki by specifically providing microcrystalline silicon TFTs comprising silicon crystallites of size 40 nm-140nm in an amorphous silicon matrix for the purpose of producing a display with TFTs easily and reliably (paragraph 11).

(10) Response to Argument

Claim 1

The Applicant argues [Appeal pages 13-14] that if transistor Q302 in Sanford were moved to be directly connected to the anode of the display element 320 then Q302 would not operate as intended by Sanford. Applicant thus argues that if Koyama were used to modify Sanford then the resulting device would be inoperable. Applicant argues that since shifting the transistor Q302 to be directly connected to the anode of the display element 320 would render the transistor Q302 inoperative for counteracting the voltage increase from transistor Q301, this modification is non-obvious.

The Examiner respectfully disagrees.

While Sanford does not teach that the second transistor Q302 is directly physically connected to the anode of the display element, Sanford does disclose that the transistor Q302 is directly <u>electrically</u> connected to the anode of the display element through transistor Q303 when transistor Q303 is turned on (column 6 lines 28-41; figure 3). When transistor Q303 is turned on to drive the display element 320, the transistor Q302 is directly electrically connected to the anode of the display element 320. Hence the transistor Q302 is <u>already</u> directly connected to the anode of the display element as

in the claims, and thus the combination with Koyama would be operable and so therefore would be an obvious combination. This is the case because the Examiner is utilizing Koyama in the claim rejection as an example of the concept of having a transistor directly connected to an anode of the display element for controlling any voltage supplied to the anode of the display element, including a holding or driving voltage, for example. The transistor 1409 in Koyama is clearly directly connected to the anode of the display element.

Further, as stated previously, the Examiner was not suggesting that the transistor Q302 be modified in any way, as the transistor Q302 is already directly connected to the anode of the display element through transistor Q303. Rather the Examiner contends that the concept of having a transistor directly physically connected to the anode of the display element is well known in the art as taught by Koyama, and that Q302, which is already directly electrically connected to the anode of the display element 320, could supply the holding voltage to the anode of the display through transistor 1409 of Koyama. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In the instant case, the Examiner is merely suggesting that by directly connecting the additional transistor 1409 from Koyama to the anode of the EL element 1405 to supply any voltage including a holding voltage to the OLED precise

gradation display can be achieved and picture quality can be improved. The Examiner is not suggesting that the transistor Q302 from Sanford be reconfigured to be directly connected to the anode of the OLED but that the concept of directly connecting a transistor to the anode of the display element for the purpose of controlling voltage is well known and would have been obvious at the time the invention was made.

The Applicant argues [Appeal pages 15-17] that Koyama does not disclose transistor 1409 for improving the quality of the display, and that the arguments in the Advisory Action are suggesting that an additional power line is necessary in the combination of Sanford and Koyama. Further Applicant argues that there must be motivation for this additional power line.

The Examiner respectfully disagrees.

Koyama clearly states in paragraphs 131-132 and specifically in paragraph 139 lines 1-4, that power control transistor 112 in figure 3 (which is the equivalent of power control transistor 1409 in figure 4 and performs the same function as transistor 1409 in figure 4A) is used to precisely control the current and voltage to the display element, which would improve the quality of the display. Further no where in the Advisory Action is it suggested or implied that it is necessary to have an additional power source control line in order to have a transistor directly connected to the anode of the display element. The embodiment of figure 4A in Koyama does have adjacent pixels that share a power source control line, but this fact has nothing to do with the function of the power control transistor 1409 within each pixel circuit, or with any claimed limitation. Other embodiments of Koyama include the same power control transistor and control it using

various methods. Further because this power source control line is nowhere in the claims, and was not used in a combination in any way, the Examiner refutes Applicant's assertion that "there must be specific principle that would motivate a skilled artisan...to add a further power supply line."

Accordingly, the Examiner respectfully submits that Applicant's arguments concerning claim 1 are not persuasive.

Claims 3-7

The Examiner respectfully submits that the Applicant's arguments regarding the above claims are not persuasive for the same reasons provided in the response to the arguments with respect to claim 1.

Claim 8

The Examiner respectfully submits that the Applicant's arguments regarding the above claim is not persuasive for the same reasons provided in the response to the arguments with respect to claim 1.

Claims 9-13 and 16

The Examiner respectfully submits that the Applicant's arguments regarding the above claims are not persuasive for the same reasons provided in the response to the arguments with respect to claim 1.

Claim 14

The Examiner respectfully submits that the Applicant's arguments regarding the above claim is not persuasive for the same reasons provided in the response to the arguments with respect to claim 1.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Stuart McCommas/
Examiner, Art Unit 2629
March 25, 2009

Conferees:

/Sumati Lefkowitz/
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/Amr Awad/
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